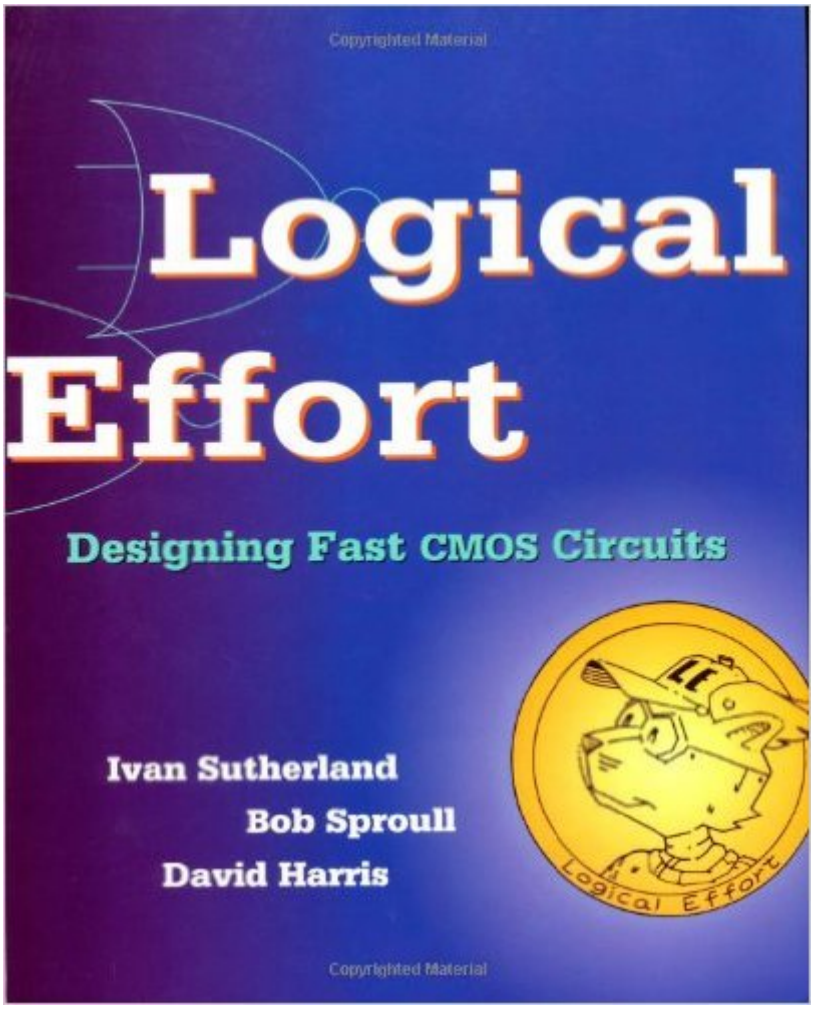
Logical Effort: Designing Fast CMOS Circuits (The Morgan Kaufmann Series In Computer Architecture And Design)



Synopsis

Designers of high-speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets. Logical Effort: Designing Fast CMOS Circuits makes high speed design easier and more methodical, providing a simple and broadly applicable method for estimating the delay resulting from factors such as topology, capacitance, and gate sizes.The brainchild of circuit and computer graphics pioneers Ivan Sutherland and Bob Sproull, "logical effort" will change the way you approach design challenges. This book begins by equipping you with a sound understanding of the method's essential procedures and concepts-so you can start using it immediately. Later chapters explore the theory and finer points of the method and detail its specialized applications. * Explains the method and how to apply it in two practically focused chapters.* Improves circuit design intuition by teaching simple ways to discern the consequences of topology and gate size decisions.* Offers easy ways to choose the fastest circuit from among an array of potential circuit designs.* Reduces the time spent on tweaking and simulations-so you can rapidly settle on a good design.* Offers in-depth coverage of specialized areas of application for logical effort: skewed or unbalanced gates, other circuit families (including pseudo-NMOS and domino), wide structures such as decoders, and irregularly forking circuits.* Presents a complete derivation of the method-so you see how and why it works.

Book Information

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Customer Reviews

This book is a long overdue explanation of the "Logical Effort" approach to MOS circuit design invented by two of the authors, Sutherland and Sproull, in the late 80's. The technique presented is complete and powerful, and this book should be required reading for all persons involved in high-performance or low-power MOS digital design. Nevertheless, I would not recommend it for beginners without some of what the authors call "instruction from veteran designers." The main shortcoming of the book is a lack of organization---important points are sometimes made in seemingly unrelated sections, and the sections themselves do not always appear to follow the most logical arrangement---and it could stand a more thorough editing job to clean up some of the presentation. Sometimes, I felt that information that was presented in charts would have been much more powerful in graph form. A few of the graphs in the book are misleading (arbitrary scales and unmarked breaks in scales), and some of the mathematical terminology is imprecise. The fact that the authors picked, somewhat arbitrarily, a new definition of the technology delay parameter tau (instead of sticking to the definition established by Mead & Conway in their 1980 book) is annoying. Aspiring asynchronous designers should be cautioned that the two designs for an n-input Muller C-element contrasted in Section 11.2 are logically different. A section contrasting the uses of the logical effort method in synchronous and asynchronous designs would also be welcome. All in all, however, the book is very readable, and it is easy to follow. It would be effective as a textbook, and it is a most welcome addition to my library because it treats a difficult and important topic better and in more detail than any other published work.

This book clarifies the method of sizing the CMOS logic gates and evaluating the different topologies of CMOS gates. Rather than solving the MOS I-V characteristic curves, it provides very intuitive, and straightforward method of estimating the propagation delay. You will find yourself a lot logically thinking about sizing CMOS gates than before when you just try to tweak the numbers and repeat simulations.

This is without a doubt a must-have for CMOS logic and circuit designers. No doubt this will be on my desk for the forseeable future. The first two chapters present a basic introduction to the approach that is sufficient to gain a working knowledge. The remaining chapters delve into details such as applying the method to domino circuits, passgate logic, cells with unequal rise/fall times, and a complete derivation of the method. The authors are well known experts in the field of high speed circuit design, and David Harris' presentation of the material is far from bland and boring.

This is one of the few technical books I had a hard time putting down. Highly recommended!

This book was really easy to read and explained the concepts well in some areas. Part of this is because my professor followed this book closely and synced it with his lectures. There were some areas that were very difficult to fully grasp without his lectures. One thing the book failed to do was fully describe assymetric sizing. They only described two input gates but never went into three input gates which is a little more tricky. There are other topics where more information would have been helpful.

Theory on the sizing of CMOS gates, written in a fun and readable manner by David Harris (from Harvey Mudd, prev at Stanford/MIT). I found it useful when I was getting started with designing circuits for custom microprocessors, because it helps to know the limits of speedup that transistor sizing can give, and Logical-Effort is a very useful framework to understand the tradeoffs.

I am currently doing a Masters degree in VLSI, and although this is not on the required book list, after trying endless parametric simulations of critical path device sizes, and trying to find the minimum delay, I found Logical efforts to be a much more elegant approach to doing that. Although some other books discuss it in minimal detail, there is no mention of if the same can be extended to other logic families other than Static CMOS. I went through a few pages of the book, and decide it to be a must buy. I also thought it was pretty cheap for 60$. Unfortunately, the book is pretty small - it’s not like a 500 page book which I was expecting it to be.I am yet to read through the whole book (which I plan to - very soon), and shall update this review once I am done with that. But I am expecting it to be worth the every cent I paid for it.

A welcome addition to the field of VLSI with pratical and not ridiculous constraints to establish fast and efficient logic designs. The book could use some introduction topics in VLSI to make the book more broad and probably more appealing as a textbook.

One of the best texts out there concerning a good way to judge a design in terms of its delay. Previous texts in VLSI have failed to really adequately describe how to address a design for optimum delay. This book makes up for this lack of content. A must read for anyone concerned with VLSI circuit design! Plus, its lots of fun to play with.

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